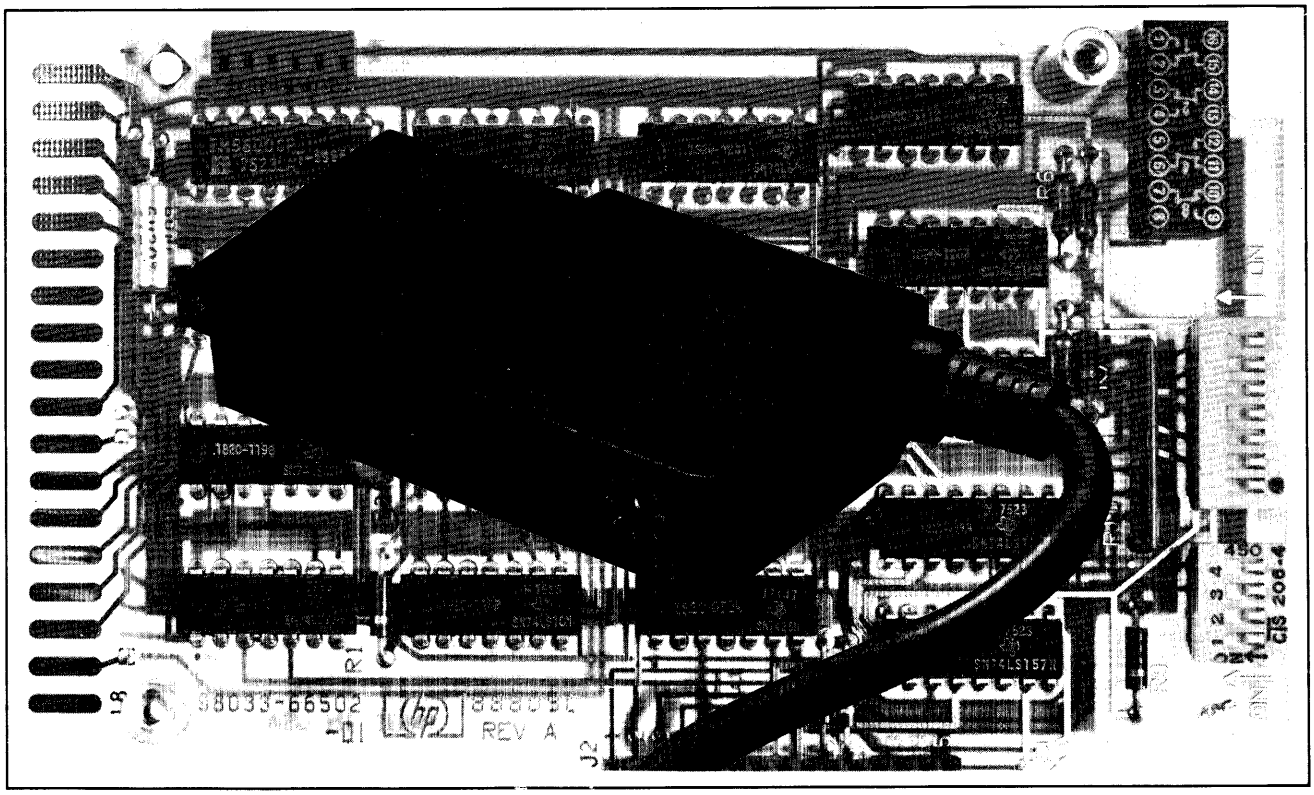
Hewlett-Packard 98033A BCD Interface
Installation and Service Manual



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98033A BCD Interface
Installation and Service Manual

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3404 East Harmony Road, Fort Collins, Colorado 80525
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Table of Contents

Chapter 4: Theory of Operation

Chapter 5: Troubleshooting and Repair

Tables

Figures

Chapter 1
General Information

Introduction

The 98033A BCD Interface provides the Desktop Computer with capability to interface a variety of instruments which have BCD information presented in bit-parallel, digit-parallel form.

The interface contains circuits which, upon execution of a read command, triggers a device to initiate a reading, waits for the device to signal that the data is available to read, and then transfers the BCD data to the calculator in the form of 16 consecutive ASCII Characters. In addition, the interface will operate in a mode which provides hardware interrupt capability.

Technical Specifications

Power Requirements:

+5 volts at 210 mA (supplied by the computer)

Operating Temperature Range:

0° C to 45° C

Signal Requirements:

1-2-4-8 BCD data
Positive or Negative true logic
Digits 0-9

Special Characters:

Binary Representation	ASCII Character
1010	(L.F.) Line Feed
1011	(+) Plus Sign
1100	(,) Comma
1101	(−) Minus Sign
1110	(E) Exponent
1111	(.) Decimal Point

Data Inputs:

Data must be stable on input while the computer is reading (data is not buffered).

All data input lines are Low Power Schottky TTL:

Min. "high" voltage	2 V
Max. "low" voltage	0.8 V
Max. input voltage	7 V
Max. low-level input current	−0.4 mA
Max. high-level input current	20 μA

Control Output Lines:

15 volt open collectors
Pull-up resistor 2.2 kΩ to +5 V
Maximum low level current: 14 mA

Peripheral Flag Lines:

Filtered, time constant ≥1 μsec.
Pull-up resistor 2.2 kΩ to +5 V
Maximum low-level input current −3.0 na

Data Rate:

Data rate is strictly dependent on the speed of the device being interfaced and the computer being used.

Dimensions:

Approximately 16.3 × 8.9 × 3.8 cm (6.4 × 3.5 × 1.5 in)

Physical Description

The 98033A BCD Interface consists of two housings which are plugged together to form a complete interface. Figure 1-1 illustrates the interface.

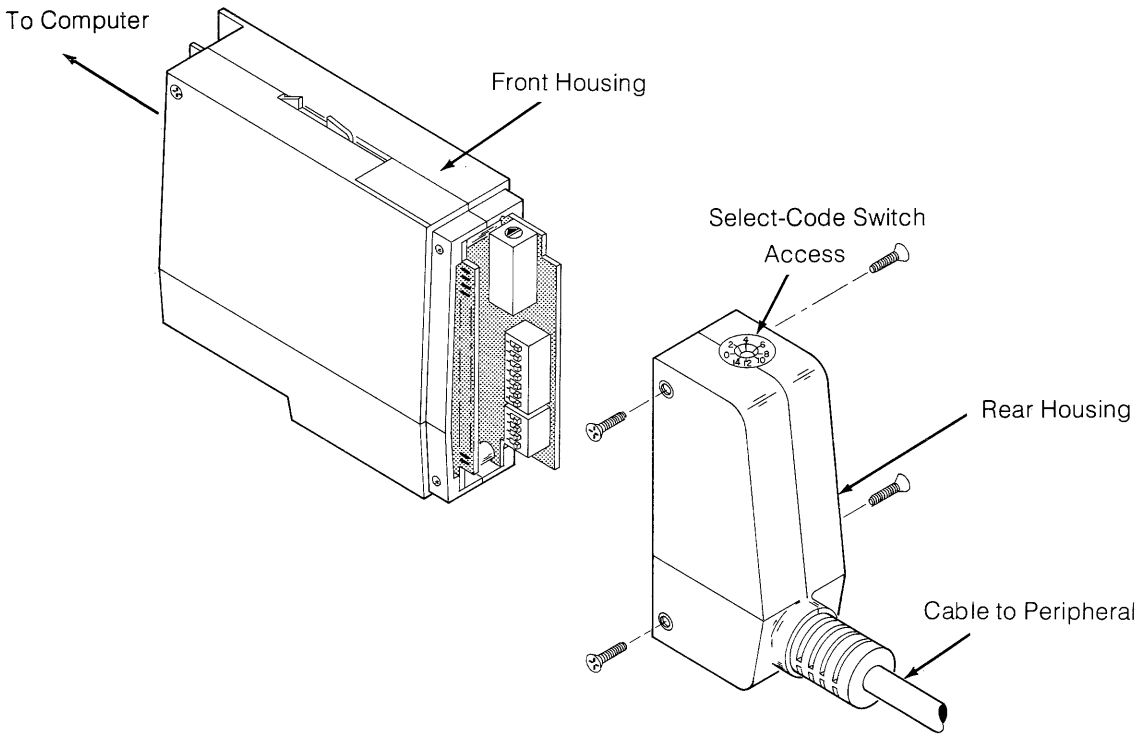


Figure 1-1. 98033A BCD Interface

Front Housing

The front housing, which plugs into the computer, is a molded case containing two printed circuit boards. These two boards comprise the circuit for the interface. One of the boards has a 2 x 18 edge-type connector at one end which connects the interface to the I/O bus of the computer. On the opposite end of the card are located the select-code switch and two sets of configuration switches.

The other board has a 2 × 25 edge connector on the back edge, which connects with the device cable in the rear housing.

Rear Housing

The rear housing is a molded case which contains the connector where the device cable is terminated.

Extending from the rear housing is a shielded cable of 48 wires, size 26; 1 wire, size 20. This cable may be connected directly to the peripheral device via an appropriate cable connector.

Options and Accessories

The 98033A BCD Interface has no options. It is shipped with a 4.5 m (15 ft.) open ended cable.

A Test Connector (98241-67933) is available to verify hardware operation of the 98033A BCD Interface.

Chapter 2
Installation

Introduction

The 98033A BCD Interface is shipped from the factory with an unterminated cable. This requires you to install the necessary terminating connector and set the "configuration" switches before connecting your peripheral device to the calculator.

Installation Considerations

Information concerning the operation of the 98033A BCD Interface should be read and understood before attempting to install this interface (refer to Chapter 3).

Interfacing to a BCD device, or two separate devices, requires that every wire in the 50 conductor device cable be connected to the device, tied to ground, or tied to the +5V reference line. Also, the configuration switches must be set for all of the proper alternatives that are needed.

Device Cable

The 50 lines of the device cable are used for signals as shown in Table 2-1.

All data lines that are not used (e.g., leading zeros) must be tied to "0"; that is, tied to ground for positive logic or to +5V reference line for negative logic.

Table 2-1. Cable Connections

Control

Mnemonic	Wire Color
CTLA	8
DFLGA	918
CTLB	98
DFLGB	928
GND	9
+5v ref	938
SHIELD*	NC

*The shield (and drain wire) should not be connected to anything at the peripheral end.

Standard Format

Data Field	Significance	Wire Color Code			
		D (8)	C (4)	B (2)	A (1)
Sgn 1	Mantissa Sign	-	-	-	916
D1 (MSD)	Mantissa Digit 1	3	2	1	0
D2	Mantissa Digit 2	7	6	5	4
D3	Mantissa Digit 3	93	92	91	90
D4	Mantissa Digit 4	97	96	95	94
D5	Mantissa Digit 5	904	903	902	901
D6	Mantissa Digit 6	908	907	906	905
D7	Mantissa Digit 7	915	914	913	912
D8 (LSD)	Mantissa Digit 8	926	925	924	923
(E)	Enter Exponent*	-	-	-	-
Sgn 2	Exponent Sign	-	-	-	917
D9	Exponent Digit	937	936	935	934
(,)	End of Value*	-	-	-	-
(O.L.)	Overload	927	-	-	-
D10	Function Code	948	947	946	945
(L.F.)	End of Reading*	-	-	-	-

*These characters are generated by the interface.
MSD – Most Significant Digit
LSD – Least Significant Digit

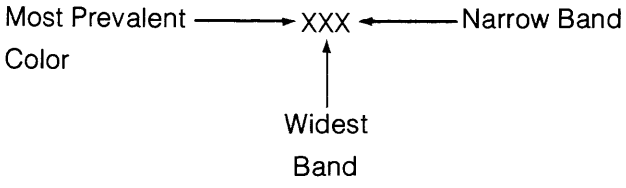
Table 2-1. (cont'd.)

Optional Format

Data Field	Significance	Wire Color Code D (8)	C (4)	B (2)	A (1)
Sgn 1	Value A Sign	-	-	-	916
D4 (MSD)	Value A Digit 1	97	96	95	94
D2	Value A Digit 2	7	6	5	4
D6	Value A Digit 3	908	907	906	905
D8 (LSD)	Value A Digit 4	926	925	924	923
(,)	End of Value A*	-	-	-	-
Sgn 2	Value B Sign	-	-	-	917
D10 (MSD)	Value B Digit 1	948	947	946	945
D1	Value B Digit 2	3	2	1	0
D5	Value B Digit 3	904	903	902	901
D3	Value B Digit 4	93	92	91	90
D7 (LSD)	Value B Digit 5	915	914	913	912
(E)	Enter Exponent*	-	-	-	-
(O.L.)	Overload A	927	-	-	-
D9	Overload B	937	936	935	934
(L.F.)	End of Reading*	-	-	-	-

*These characters are generated by the interface.
MSD – Most Significant Digit
LSD – Least Significant Digit

Wire color codes shown correspond to the standard resistor color code. Digits have the following significance:

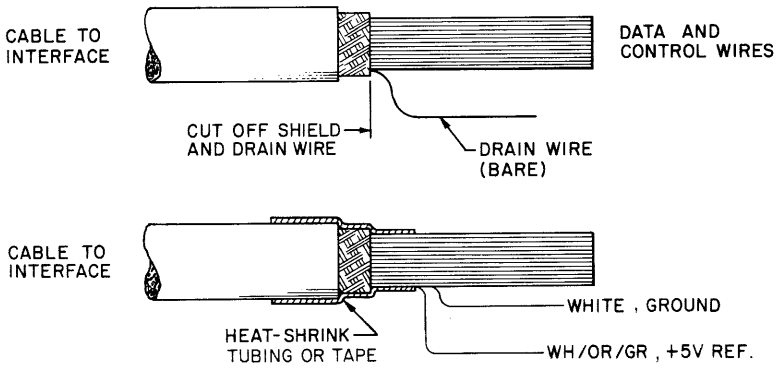


0 - Black
1 - Brown
2 - Red
3 - Orange
4 - Yellow
5 - Green
6 - Blue
7 - Violet
8 - Gray
9 - White

Unused data lines should be connected to either the +5V ref wire (938) or to the ground wire (9), depending on the ASCII character you want in the unused data field (refer to Table 2-2).

If only one device is being interfaced, the unused control and flag lines (i.e., CTLB and DFLGB) should be connected to one another and isolated. All configuration switches which affect these signals should be left OFF.

The shield and drain wire (bare wire) should be cut off and not used for a ground. The logic ground to be used is the GND wire (9) (refer to Figure 2-1).



Select Codes

The select code should be checked for the proper setting as required by your system. The select-code switch is accessible through a hole in the top of the rear housing. The interface will be preset, at the factory, to select code 3. If it is necessary to change the setting, rotate the switch to the desired position, using a small screwdriver.

You should avoid using select codes reserved for the peripherals internal to the computer. Refer to the Operating and Programming Manual supplied with your Desktop Computer for a listing of reserved select codes.

Two interfaces should not be set to the same select code.

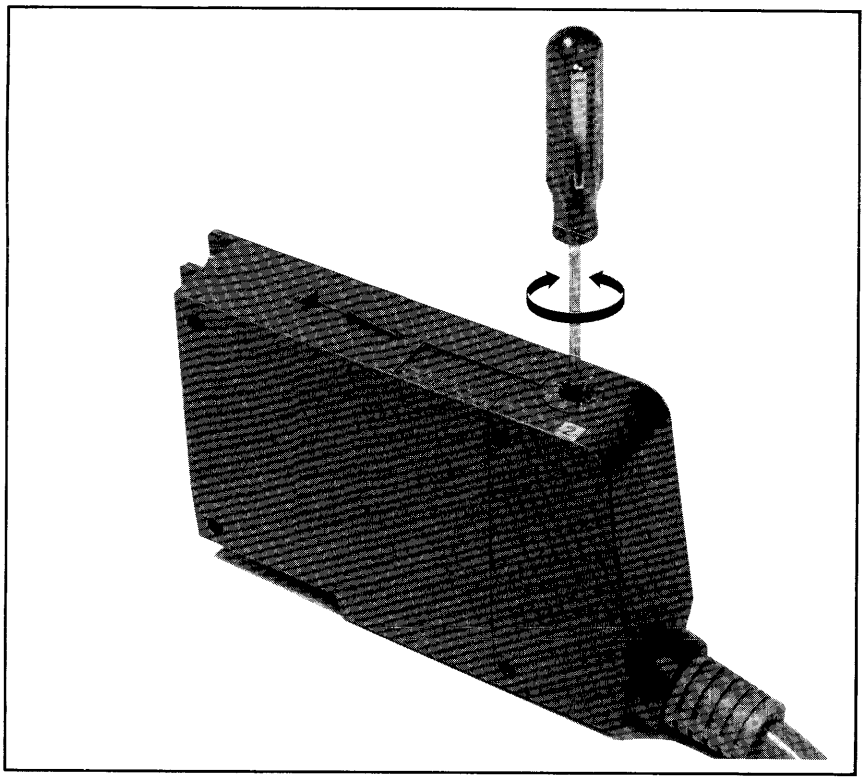


Figure 2-2. Setting the Select-Code Switch

Select Code Interrupt Considerations*

Select codes 0 through 7 are on the low priority interrupt level and select codes 8 through 15 are on the high priority level. Devices requiring fast interrupt service should be set to the high level. Priority within a level is in order of the select code, with 7 and 15 having the highest priority.

*An I/O ROM with interrupt capability is required to use the interrupt mode, refer to the appropriate ROM manual.

Configuration Switches

The configuration switches determine the interface's mode of operation. These switches are accessed by removing two screws from each side of the interface and then removing the rear housing. The modes controlled by the switches may be considered in four separate groups, each group is described in the following sections.

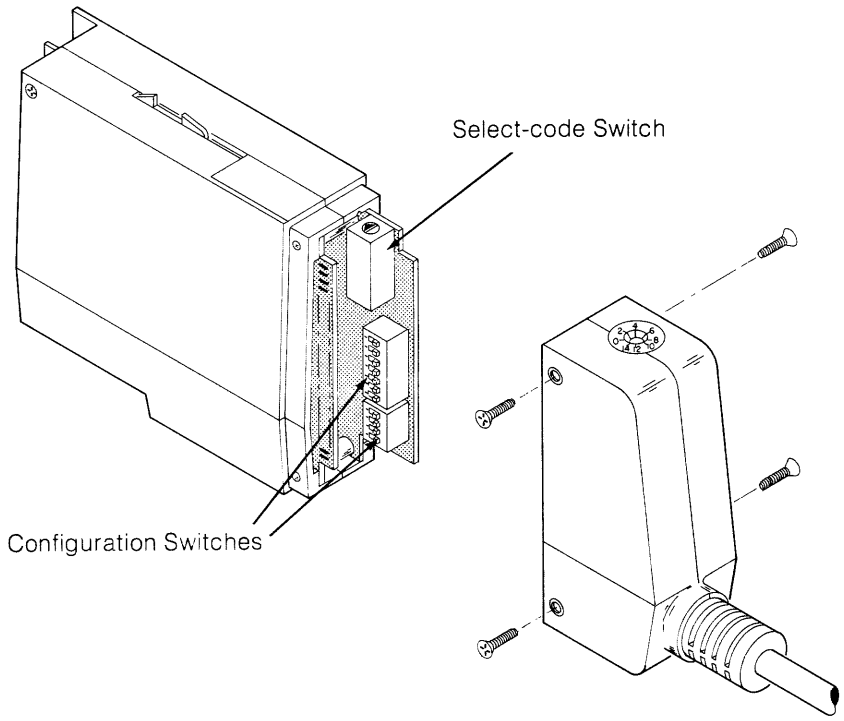


Figure 2-3. Configuration Switch Locations

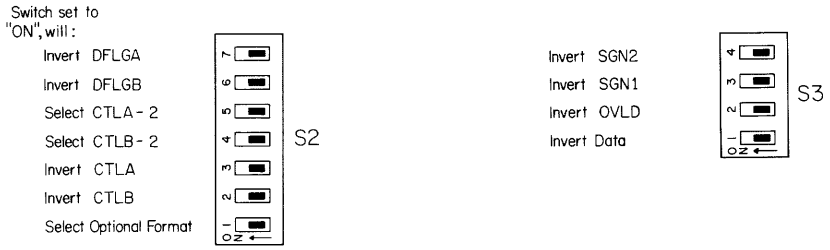


Figure 2-4. Configuration Switches

Data Inversion

When set to ON, the inversion switches for SGN1, SGN2, and OVLD causes each of these signals to be inverted before they are multiplexed and transferred to the computer.

The invert-data switch when set to ON causes all data to be inverted after it has been multiplexed. Thus, if SGN1, for example, was inverted, it would be inverted again before being transferred to the computer.

The normal logical sense (switch in the OFF position) for input data is listed below:

D1-D10: positive BCD (1 = +5v, 0 = ground)
SGN1, SGN2: 0 = plus (+), 1 = minus (−)
OVLD: 0 = no overload, 1 = overload

Handshake Inversions

If the logical sense of any of the handshake signals needs to be inverted, the respective switches to invert CTLA, CTLB, DFLGA, or DFLGB may be set to ON. The normal sense of these signals may be seen in Figure 2-5. CTLB and DFLGB have the same sense as CTLA and DFLGA respectively.

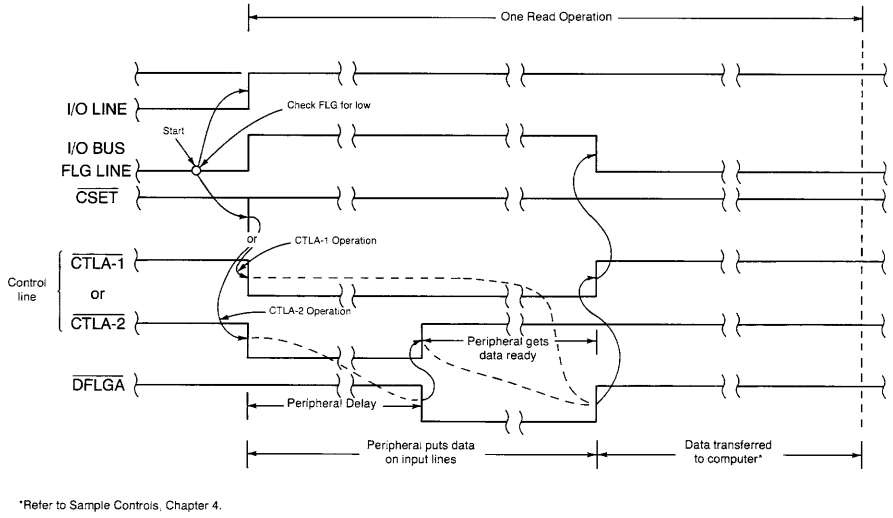


Figure 2-5. CTLA-1 and CTLA-2 Timing

Control Options

If the form of control shown in Figure 2-5 as CTLA-1 is not suitable for an application, the CTLA-2 (or CTLB-2) option switches may be set to ON to give a control signal of the form of CTLA-2 (a pulse type operation).

Format Options

The format option switch may be set to select either the standard format (switch OFF) or the optional format (switch ON); refer to Chapter 3.

Input Formats

The following table shows the relationship between the BCD Codes and the ASCII characters that are available from this interface.

Table 2-2. BCD Code to ASCII Character

BCD Code		ASCII Character
Positive True Logic	Negative True Logic	
0000	1111	0
0001	1110	1
0010	1101	2
0011	1100	3
0100	1011	4
0101	1010	5
0110	1001	6
0111	1000	7
1000	0111	8
1001	0110	9
1010	0101	(L.F.) Line Feed
1011	0100	(+) Plus
1100	0011	(,) Comma
1101	0010	(−) Minus
1110	0001	(E) Exponent
1111	0000	(.) Decimal Point

Data Fields

The ten, 4-bit data fields, D1-D10, may be connected to any 4-bit BCD output digit on a device or may be permanently wired to represent any of the characers available on the interface (see Table 2-2). For example, if a decimal point is needed in the D5 data field, all 4 wires of D5 (D5-A, D5-B, D5-C, and D5-D) should be tied to +5V reference line (grounded for negative logic).

Overload and Signs

The remaining three data fields (OVLD, SGN1, and SGN2) are more limited data fields since only one signal line is available for each. OVLD may take on two values: 0 when overload does not exist, and 8 when overload does exist. A switch is provided which will invert the logical sense of OVLD.

Similarly, the SGN1 and SGN2 fields may represent two characters each: plus (+) when the line is low, and minus (−) when the line is high. Switches are used to change this logical sense, as with OVLD.

Control and Flag Lines

The remaining four lines in the device cable are the CTLA, CTLB, DFLGA, and DFLGB lines. These lines carry the "handshakes" performed between the interface and the device(s). The control lines, CTLA and CTLB, should be connected to the external trigger (encode, start conversion, etc.) terminals of devices A and B* respectively. Similarly, the flag lines, DFLGA and DFLGB, should be connected to the data ready (print command, end of conversion, etc.) terminals of the respective devices.

If only one device is being interfaced, the other CTL line and DFLG line must be connected together and isolated.

If inversions are required on either CTLA or CTLB or on DFLGA or DFLGB, the appropriate configuration switch must be set to ON. If the form of CTLA (or CTLB) needs to be changed from CTLA-1 to CTLA-2 the appropriate configuration switch must be set to ON. Figure 2-5 shows the form of CTLA-1 and CTLA-2.

*Refer to Optional Format, Chapter 3.

Recommended Driver and Receiver Circuits

It is recommended that all inputs used on the interface (including DFLGA and DFLGB) be driven with TTL logic, or with open-collector drivers as shown in Figure 2-6. The receivers shown in Figure 2-7 are recommended for CTLA and CTLB.

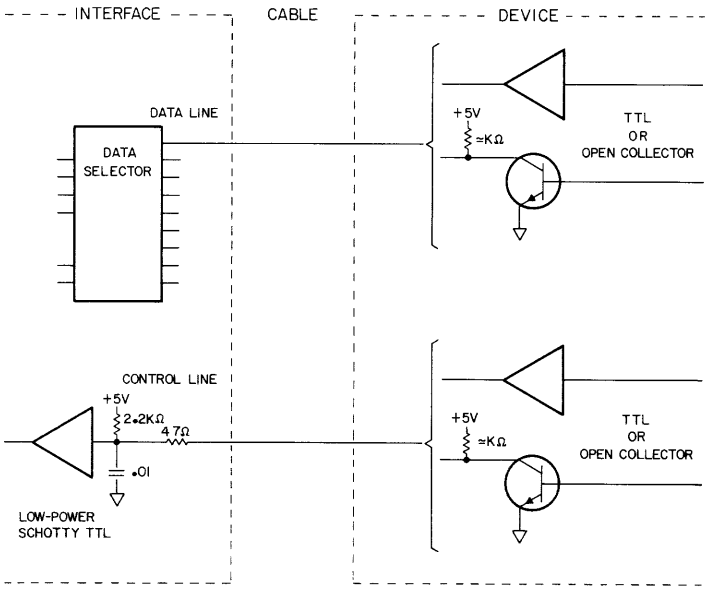


Figure 2-6. Recommended Drivers

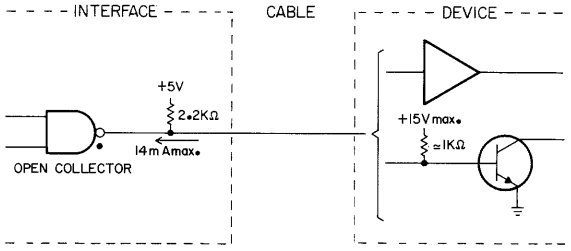


Figure 2-7. Recommended Receiver

Chapter 3
Operation

Introduction

There are two modes of operation of this interface; they are referred to as "general" and "interrupt".

General Operation

In general operation, when the computer executes an input operation, the interface triggers the device to initiate a reading and waits for the device to signal that the data is available to be read. The interface accepts the BCD data and transfers it to the computer in the form of 16 consecutive ASCII characters. The data may be transferred to the computer in one of two formats, "Standard" or "Optional."

Standard Format

The standard format is designed to allow the computer to read up to eight significant digits from a device, a one-digit exponent (power of ten), two signs, and overload digit, and a one digit function code. This format would be received by the computer as:

Data Field 1 2 3 4 5 6 7 8 9 10

(±) X X X X X X X X E (±) X , (O.L.) X (L.F.) Refer to Table 2-1.

MSD thru LSD

Where:

(±) – is an ASCII plus or minus, depending on the logic level of the SGN Signal from the device.

X – denotes a character which corresponds to a full 4-bit BCD Code (0-9 or special characters) from a device.

E – is an ASCII "E" which marks the beginning of an exponent.

(,) – is an ASCII comma which marks the end of the first value.

(O.L.) – is an ASCII "8" when overload exists, and "0" when overload does not exist.

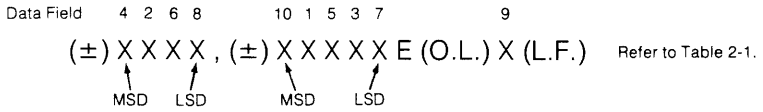
(L.F.) – is an ASCII line feed which marks the end of the second value.

This format is suitable for reading a data value, and then a function code from a single device.

Optional Format

The optional format will facilitate reading from two devices through a single interface. This format allows the interface to read up to four digits from one device and up to five digits from a second device, along with a sign and an overload indicator from each. To provide this capability of reading from two devices, there are two separate sample control circuits on the interface, which separately detect when each device has data ready.

The optional format presents characters to the computer in the following sequence.



The symbols have the same meaning as with the standard format.

Interrupt Operation

If the device(s) being interfaced is very slow and it is desired that the computer perform useful work while the device is busy, interrupt operation is available. While in the interrupt mode, the interface requests service from the computer when data is available to be read.

An I/O ROM with interrupt commands is required to use the interrupt capability; refer to the appropriate ROM Manual.

Interface Reset

The interface can be reset under program control using an R5 OUT (wtc, WRITE IO <sc>,5;) operation. For example, using the 9825A computer, a `wtc<s.c.>; 32` would reset the interface at the select code indicated. In BASIC, the statements `RESET<sc>` or `WRITE IO<sc>;5; 32` can be used.

Example of Operation

The following examples show HPL and BASIC syntax.

Standard Format

When the interface is configured for standard format, a read statement will cause a reading to be taken. The statement, `ENTER 3;A,B` / `red 3, A, B` could result in the following:

	A	B
Transfers -	+00031.64E−3	,02(L.F.)
A Contents -	3.164E−2 : value	
B Contents -	2.0: function code	

Optional Format

Configuring the interface for the optional format and performing a `ENTER 3;A,B` / `red 3, A, B` might result in a reading like this from two devices:

	A	B
Transfers -	+1234	,56789E00(L.F.)
A Contents -	1.234E3 : Value A	
B Contents -	5.6789E4 : Value B	

Overload Detection

With the standard format example, a function code (B Contents), greater than 80, would indicate an overload.

With the optional format example, the overload information could be contained in the exponent of Value B. For the various combinations possible we would see the exponent take on the following values.

E00 - no overload
E80 - device A overloaded
E08 - device B overloaded
E88 - both devices overloaded

Chapter 4
Theory of Operation

Introduction

The Theory of Operation is presented in two sections.

1. Computer I/O Backplane
2. Block Diagram Description

The Computer I/O Backplane section is given to provide better understanding of the interaction between the computer and the interface.

Computer I/O Backplane

The following table lists the mnemonic and a brief description of the lines available at each of the computer I/O slots.

Table 4-1. Computer Backplane Signals

Signal	Direction Calc. ←→ Interface	Description
$\overline{IOD0}$-$\overline{IOD7}$	←→	Input/Output data lines
$\overline{PA0}$-$\overline{PA3}$	→	Peripheral address, range: 0-15
$\overline{INIT}$	→	Calculator Initialize (reset)
$\overline{IC1}$, $\overline{IC2}$	→	Register code lines, R4-R7
$\overline{IOSB}$	→	Input/Output strobe line
$\overline{DOUT}$	→	Direction of transfer
$\overline{STS}$	←	Interface status line, 1=interface present
$\overline{FLG}$	←	Interface flag line, 1=interface free
$\overline{IRH}$	←	Request service, address from 8 to 15
$\overline{IRL}$	←	Request service, address from 0 to 7
$\overline{INT}$	→	Demand response to interrupt poll

I/O Registers

The computer provides access to four I/O registers R4, R5, R6, and R7. These registers are located on the interface and are used as paths for input/output operations. Several of these registers are only virtual registers and cannot store any data.

IC1 and I C2 are the signals on the I/O backplane that indicate which register (R4-R7) is being used during the current I/O operation.

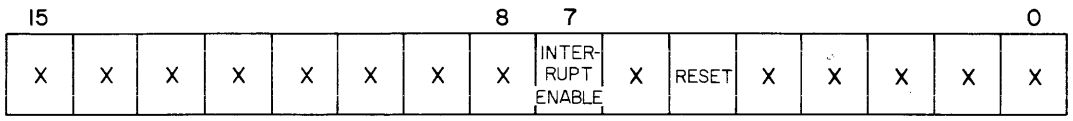
The four combinations of IC1 and IC2 and the corresponding register referenced are as follows.

$\overline{IC2}$	$\overline{IC1}$	Register
0	0	R4
0	1	R5
1	0	R6
1	1	R7

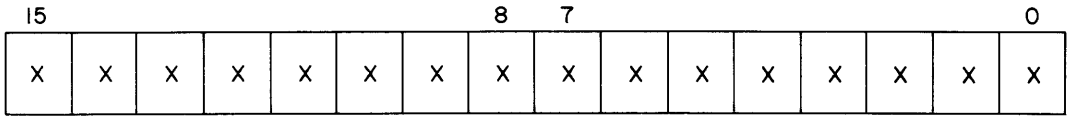
Each I/O register operation has a consistent use among the different types of interfaces. Figure 4-1 illustrates the use of registers R4-R7 on the 98033A BCD Interface.

Output Register Operations

Register 5 - Sets Status

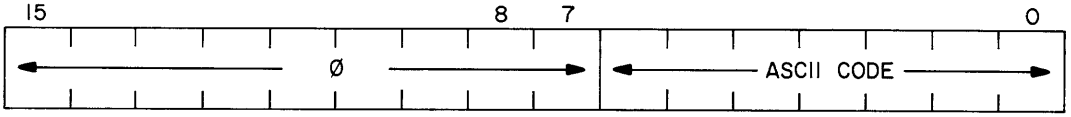


Register 7 - Demands Next Character

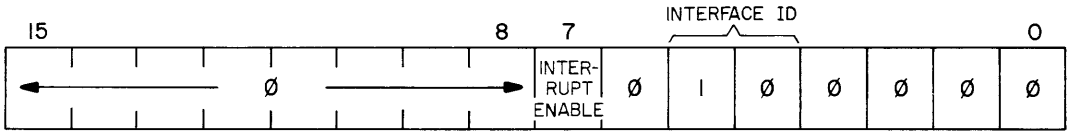


Input Register Operations

Registers 4 or 6 - Reads ASCII Character



Register 5 - Reads Status



All register operations not shown are ignored.

(X = don't care)

Figure 4-1. I/O Register Operations

Flag and Status Lines

The FLG and STS lines indicate to the computer when the interface is ready for an operation. When the interface is plugged into the computer and is addressed, STS will be low. When neither CTLA or CTLB are set (neither device is busy), the FLG line is low to show that the interface is ready for an operation.

Interface Block Diagram Description

Refer to Figure 4-11, the Block Diagram, when reading the following information. The Block Diagram shows eight functional areas in the interface.

1. Address Decoder
2. Command Decoder
3. Character Counter
4. Sample Controls
5. Multiplexer
6. Code Converter and Interrupt Poll Responder
7. Interrupt Logic
8. Reset Logic

Interface Mnemonics

The following table lists the mnemonics, with a brief description of the lines used within the interface.

Table 4-2. Interface Signals

Mnemonic	Description
D1-D10	Data Fields 1-10
D1A-D10A	Least Significant Bit of Data Field
D1B-D10B	Second Significant Bit of Data Field
D1C-D10C	Third Significant Bit of Data Field
D1D-D10D	Most Significant Bit of Data Field
SGN1, SGN2	Algebraic Sign of Data
OVLD	Overload Line
CTLA-1, CTLA-2	Two Forms of Control for Device A
CTLB-1, CTLB-2	Two Forms of Control for Device B
DFLGA	Flag from Device A
DFLGB	Flag from Device B
ADR	Interface Addressed
SSW0-SSW3	Select Code Switch Bits
HPA	High Peripheral Address Bit
R5SB	Decoded Write Status
R7SB	Decoded Demand Next Data Character
R4IN	Decoded Read Data Character
R5IN	Decoded Read Status
RST	Interface Reset
CSET	Sample Control Set Pulse
MAD A-MAD D	Multiplexer Address
IR	Interrupt Request

Address Decoder

The purpose of the Address Decoder is to determine when the interface is addressed by the computer to perform an I/O function. The interface will only respond when the 4-bit peripheral address, PA0-PA3, matches the address set on the select-code switch. If the address matches and the calculator is not conducting an interrupt poll (INT); then the interface is enabled (ADR) to look at the I/O commands.

When the conditions above are met, the interface shows its presence to the computer by grounding the status line (STS), and by taking control of the flag line (FLG) which it sets to a low state if the interface is ready to begin an operation.

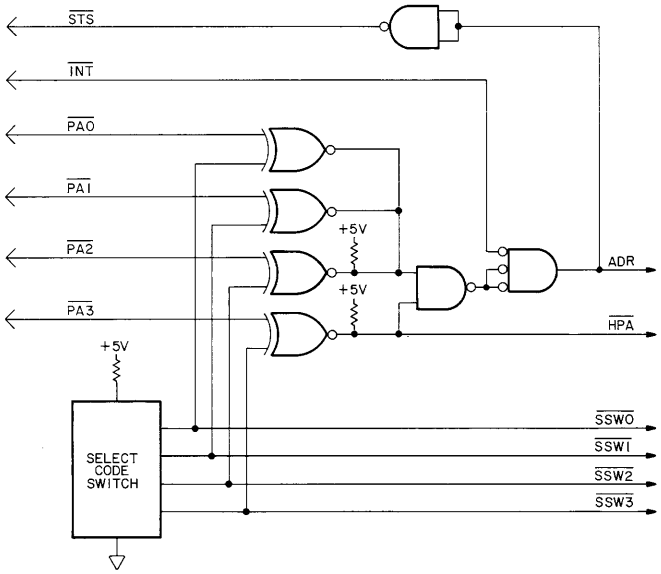


Figure 4-2. Address Decoder

Command Decoder

The Command Decoder is a network of gates which interprets the type of I/O transfer that is being demanded by the computer. It determines whether the transfer is an input or an output operation by looking at DOUT. Whether input or output, the transfer may be directed to one of four registers: R4, R5, R6, or R7. The significance of these registers is discussed in "Computer I/O Backplane." Signals IC1 and IC2 are coded to reflect which register is designated.

In addition, on output operations, the I/O strobe pulse, IOSB, is gated through the command decoder to clock status onto the interface.

The four decoded signals, R4IN, R5IN, R5SB, and R7SB, which come from the command decoder are the only commands recognized by the interface.

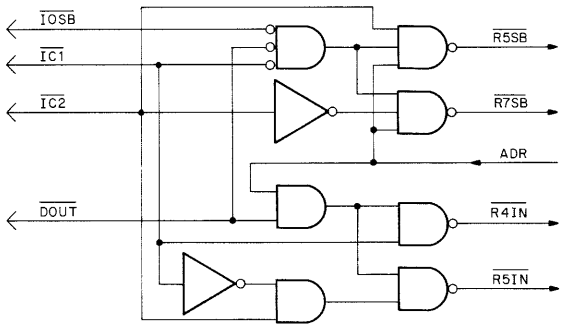


Figure 4 -3. Command Decoder

Character Counter and Format Selector

The character counter (Figure 4-4) is a synchronous-binary-down counter which serves to address the multiplexer and to initiate the device sample controls.

When the interface is initialized or reset, the character counter is in the "0" state.

During a read operation, the counter will see a series of 16 R7SB pulses, each decrementing the counter to a new multiplexer address. The very first R7SB, taking the counter from the "0" state, is gated through the counter as a borrow pulse (CSET) and is used to set both device sample controls. The last R7SB returns the counter to the "0" state. Figure 4-5 is a timing diagram showing a typical read operation.

If the standard format is selected the outputs of character counter, Q_A, Q_B, Q_C, and Q_D, are gated directly through the format selector to MADA, MADB, MADC, and MADD respectively. If the optional format is selected Q_A generates MADC, Q_C generates MADD, Q_D generates MADA; and Q_B generates MADB as with the standard format.

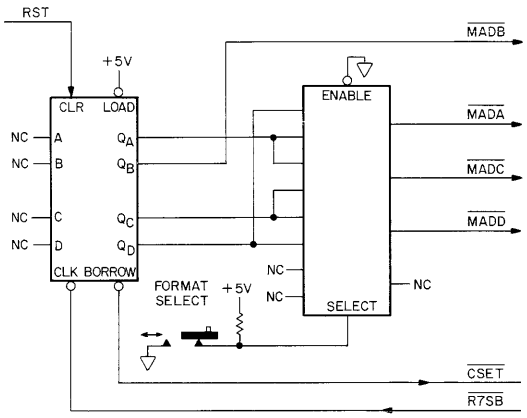
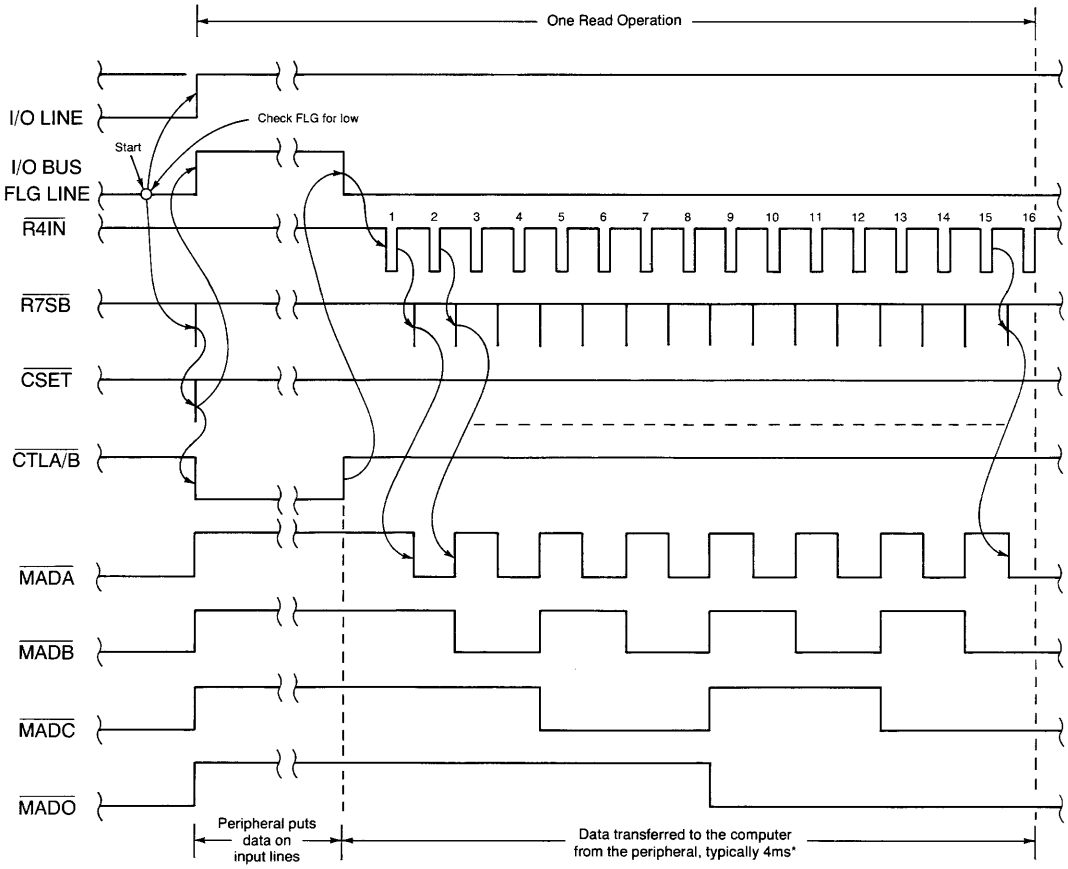


Figure 4-4. Character Counter and Format Selector



*Data must be held stable on input lines during this period (refer to the next section for timing).

Figure 4-5. Timing Diagram For a Read Operation (Standard Format)

Sample Controls

Two identical sample controls (CTLA and CTLB) are provided which may be used to initiate samples from two separate devices. One of these controls is depicted in Figure 4-6.

The control consists of a D-type flip-flop which is set by a pulse from the character counter (CSET). The control signal is seen as a low level by the device being triggered. The exclusive-or gate allows the sense of the control signal to be inverted. The open-collector drivers will withstand 15 volts and will sink 16 mA of current.

The sample control flip-flop is reset by a negative-going edge on the device flag (DFLG) line, which signals that the data is ready. The logical sense of DFLGA may be inverted so that control resets on the positive-going edge.

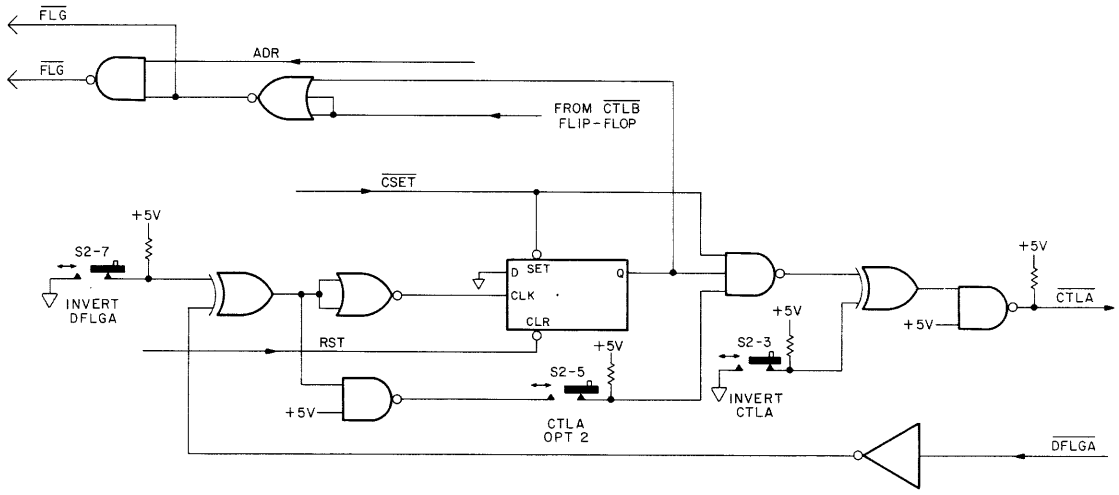


Figure 4-6. Sample Control

For some applications it is necessary that CTLA-1 be reset before device A indicates that data is ready. For these applications, a second form of control is offered, CTLA-2. When CTLA-2 is selected, control to the device is locked out after the first transition of DFLGA. Figure 4-7 is a timing diagram which shows the distinction between CTLA-1 and CTLA-2.

The time required for the data to be transferred to the computer is typically 4ms, but it could take an indefinite amount of time depending on the other computer operations. Interrupts and DMA are the types of operations that could affect the transfer time. The only absolute way to ensure that the data is transferred completely is to have the data available on the input lines until the next read operation.

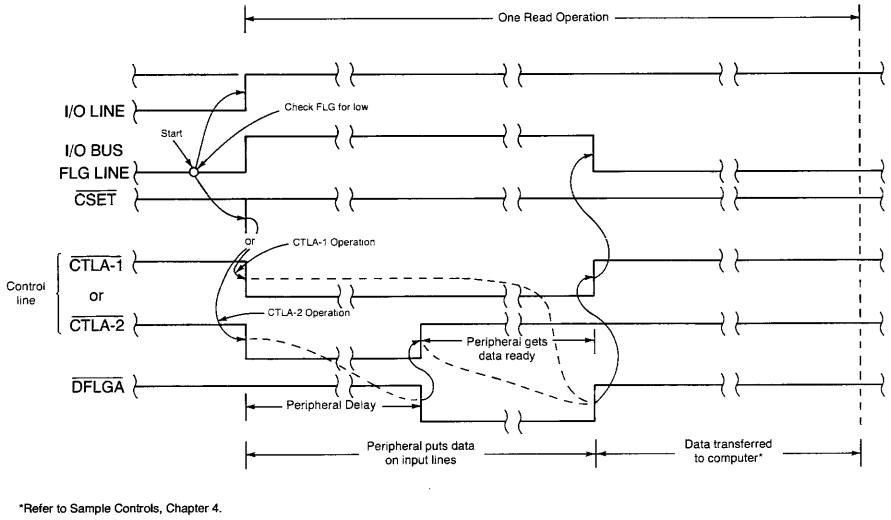


Figure 4-7. Handshake Timing Diagram

CTLB behaves the same as CTLA.

When either CTLA or CTLB is set, FLG indicates busy to the computer.

Multiplexer

The Multiplexer selects one of 16 data fields to present as data to the code converter which forms the ASCII character to be sent to the computer. The multiplexer is a one-of-sixteen word selector. Each word is a 4-bit binary representation of some digit or special code. Ten of the data fields are used to bring in actual BCD digits, D1-D10, from the peripheral devices(s); three are partially fixed and partially set by the devices: SGN1, SGN2, and OVLD; and three are fixed to special codes for the three characters L.F. (line feed), comma, and "E."

The logical sense of the OVLD, SGN1, or SGN2 signals may be inverted before they are multiplexed. Also, the logical sense of all the data may be inverted after multiplexing. The exclusive-or gates on OVLD, SGN1, and SGN2 accomplish the first inversion mentioned, while the quad one-or-two selector (U1) accomplishes the inversion of all data.

The outputs of the multiplexer are tri-state logic which allows the multiplexer to be disabled when an interrupt poll is being conducted.

The net output of the multiplexer is a sequence of 4-bit binary codes which serve as addresses for the Read Only Memory (ROM) Code Converter (U4).

Code Converter and Interrupt Poll Responder

The Code Converter and Interrupt Poll Responder generates the actual ASCII characters which are transferred to the calculator, and generates the proper response if the interface has requested interrupt service and the calculator is polling all interfaces.

This block consists largely of a 32 × 8 bit ROM which has its open-collector outputs placed directly on the calculator I/O bus (IOD0-IOD7). The contents of the ROM are listed in Table 4-3. As may be seen from the table, the first 16 locations of the ROM serve as the code converter while the first eight of the last 16 locations serve as the poll responder.

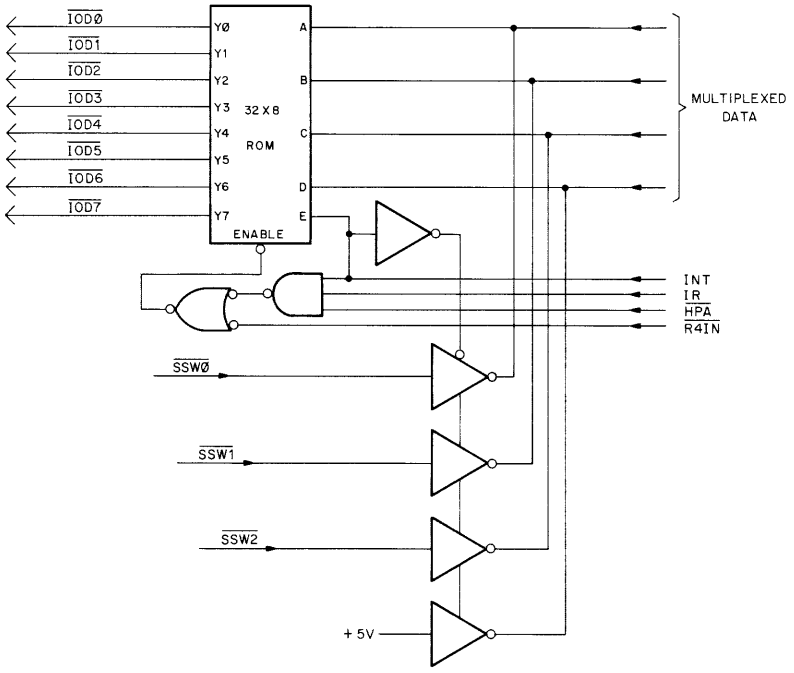


Figure 4-8. Code Converter and Interrupt Poll-Responder

Table 4-3. ROM Contents

Address		Contents		Significance	
Octal	Binary EDCBA	Octal	Binary $Y_7 \ldots\ldots Y_0$		
0	00000	60	00110000	ASCII "0"	
1	00001	61	00110001	ASCII "1"	
2	00010	62	00110010	ASCII "2"	
3	00011	63	00110011	ASCII "3"	
4	00100	64	00110100	ASCII "4"	
5	00101	65	00110101	ASCII "5"	
6	00110	66	00110110	ASCII "6"	
7	00111	67	00110111	ASCII "7"	
10	01000	70	00111000	ASCII "8"	
11	01001	71	00111001	ASCII "9"	
12	01010	12	00001010	ASCII (L.F.) line feed	
13	01011	53	00101011	ASCII (+) plus	
14	01100	54	00101100	ASCII (,) comma	
15	01101	55	00101101	ASCII (−) minus	
16	01110	105	01000101	ASCII (E) exponent	
17	01111	56	00101110	ASCII (.) decimal pt.	
20	10000	1	00000001	0 or 8	Interrupt Poll Response for Select Code
21	10001	2	00000010	1 or 9	
22	10010	4	00000100	2 or 10	
23	10011	10	00001000	3 or 11	
24	10100	20	00010000	4 or 12	
25	10101	40	00100000	5 or 13	
26	10110	100	01000000	6 or 14	
27	10111	200	10000000	7 or 15	
30	11000	0	00000000		Null
31	11001	0	00000000		
32	11010	0	00000000		
33	11011	0	00000000		
34	11100	0	00000000		
35	11101	0	00000000		
36	11110	0	00000000		
37	11111	0	00000000		

Interrupt Logic

The interrupt logic on the interface gives it the ability to request service from the computer when data is ready for the computer.

A write register 5 operation with bit 7 set to a "1" (low state) will enable the interrupt logic to operate. Similarly, a write register 5 with bit 7 set to a "0", or an interface reset, will disable the interrupt logic.

When the interrupt enable flip-flop (U17-A) is set, the interrupt logic looks at the busy indicator (FLG) which is a logical "or" of both device sample controls. If both controls are reset, the interface is not sampling and, therefore, must either have data ready to read, or be waiting to initiate another reading. In either case, the interrupt logic requests service (IR) by grounding the appropriate interrupt request line. IRL will be grounded if the select-code switch is set to an address between 0 and 7, and IRH will be grounded if the switch is set between 8 and 15.

When the computer senses a service request, it will conduct an "interrupt poll" to determine which peripheral(s) requested service. A poll is being conducted when INT is low. If PA3 matches SSW3 while INT is low, the interrupt logic will force the Interrupt Poll Responder to ground one bit on IOD0-IOD7. Which bit is grounded depends on the setting of the select-code switch as shown in Table 4-4.

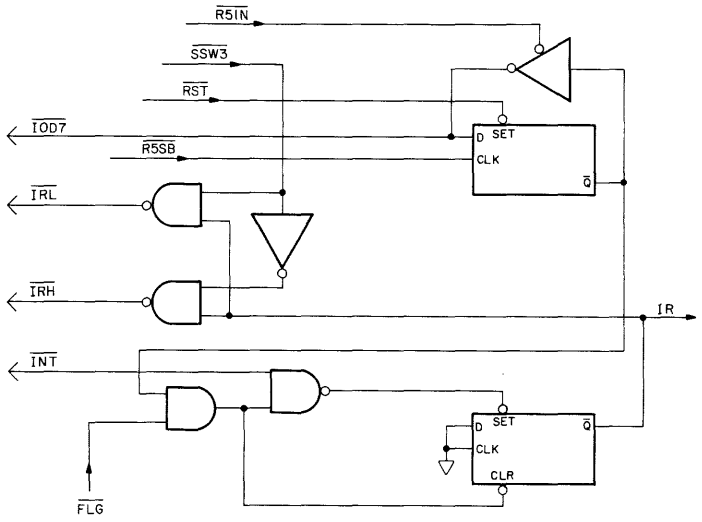


Figure 4-9. Interrupt Logic

Table 4-4. Interrupt Poll Response

Select Code Switch					Line on Data Bus that is Grounded During a Poll
SSW 3	SSW 2	SSW 1	SSW 0	Position	
0	0	0	0	0	IOD0
0	0	0	1	1	IOD1
0	0	1	0	2	IOD2
0	0	1	1	3	IOD3
0	1	0	0	4	IOD4
0	1	0	1	5	IOD5
0	1	1	0	6	IOD6
0	1	1	1	7	IOD7
1	0	0	0	8	IOD0
1	0	0	1	9	IOD1
1	0	1	0	10	IOD2
1	0	1	1	11	IOD3
1	1	0	0	12	IOD4
1	1	0	1	13	IOD5
1	1	1	0	14	IOD6
1	1	1	1	15	IOD7

Reset Logic

The remaining part of the interface is a circuit which resets the interface to a known state under either of two conditions:

- When the computer initializes the interface, INIT goes low and the character counter, device sample controls, and interrupt enable logic are reset.
- A write register 5 operation with bit 5 set to a "1" (low) has the same effect as INIT.

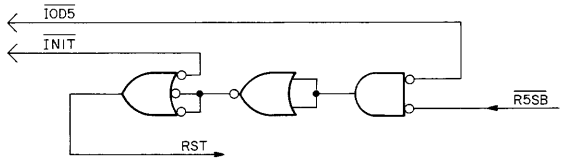


Figure 4-10. Reset Logic

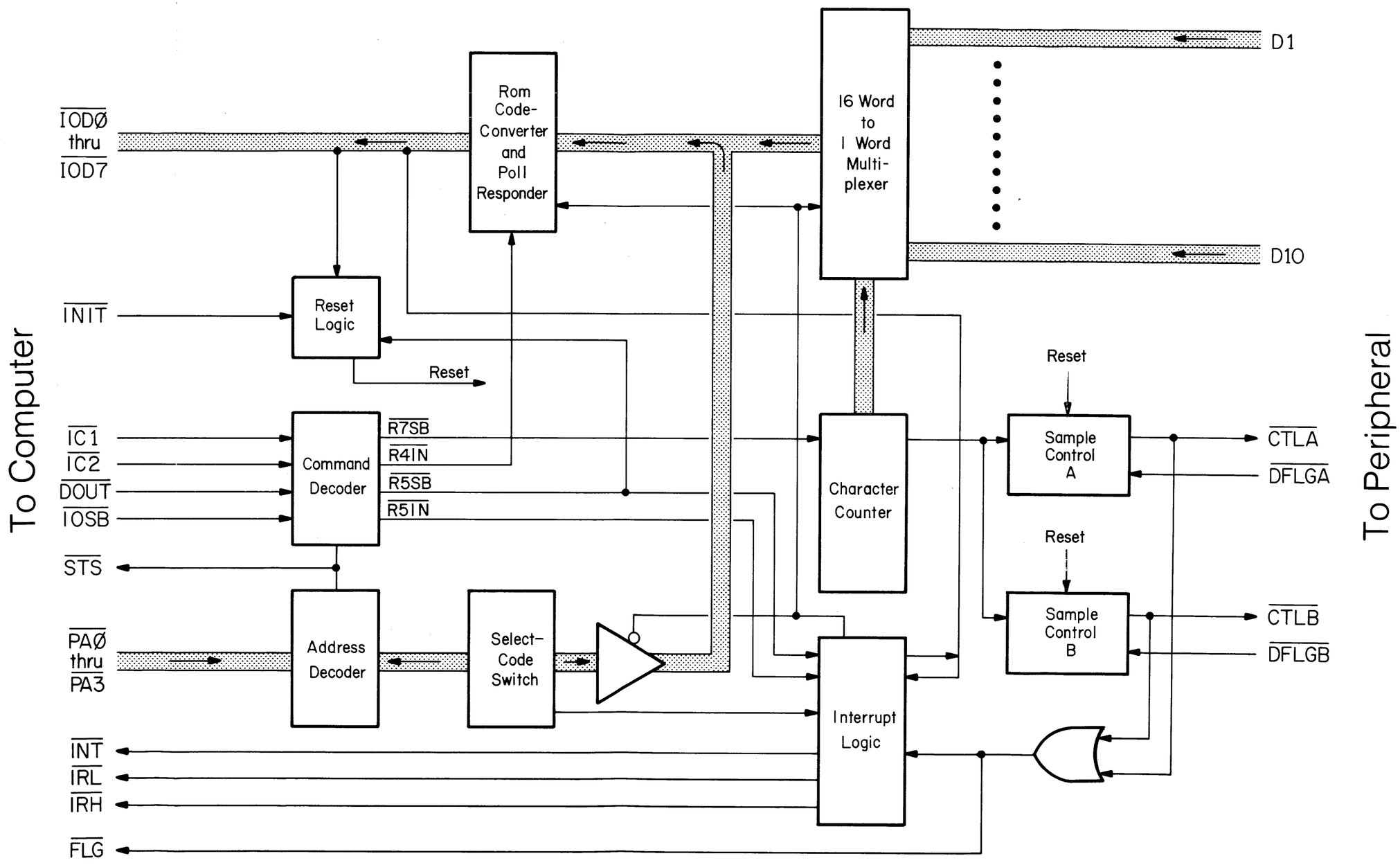


Figure 4-11. 98033A BCD Interface Block Diagram

Chapter 5
Troubleshooting and Repair

Introduction

The following procedures assume that the computer, ROM(s) and peripheral device are operating correctly. If necessary, disconnect the interface from the computer and perform all other applicable test procedures before assuming that the interface is defective.

Recommended Equipment

The following is a list of equipment that will aid in troubleshooting the 98033A BCD Interface.

1. Oscilloscope or Logic Probe
2. Test Connector 98241-67933
3. Extender Board 98241-67901
4. Computer and applicable ROM(s)

For checking most signals within the interface, any general purpose oscilloscope or logic probe can be used, if it is capable of indicating the presence of TTL level signals with pulse widths greater than 200ns.

Interface Operational Test

The following procedure shows how to test the operation of the 98033A BCD Interface.

Procedure

1. Remove the interface rear housing and install the test connector, see Figure 5-1.

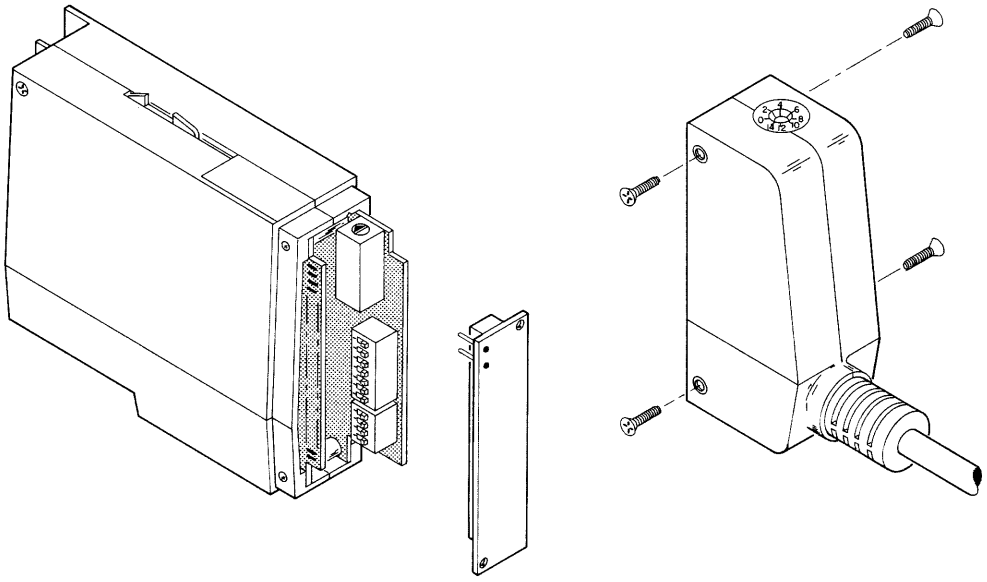


Figure 5-1. Test Connector Installation

2. Set the select code switch to 3.
3. Switch the computer on.
4. Load the appropriate test program.
5. Press RUN.
6. Change the configuration switches (see Figures 2-3 and 2-4) to each position listed in the appropriate table (5-1 or 5-2), and then press, CONTINUE.
7. Each time CONTINUE is pressed the computer display should be as shown (refer to Tables 5-1 or 5-2 for the configuration switch positions for the respective programs).
8. If each test results in the proper display the Interface is operating correctly. If no further testing is required the test connector can be removed and the rear housing re-installed.
9. If any of the tests fail re-check:
   a. the test connector installation.
   b. the interface installation.
   c. the test program.

10. If the interface continues to fail, contact the nearest HP Sales and Service Office or refer to Theory of Operation and Troubleshooting sections of this manual.

Interface Test Programs

HPL

```
0: fmt; wtc 3,32;red 3,X,Y
1: fmt 2e16.6;wrt 0,X,Y
2: stp ;eto 0
3: end
```

BASIC

```
10   WRITE IO 3,5;32
20   ENTER 3;X,Y
30   DISP X,Y
40   STOP
50   GOTO 10
60   END
```

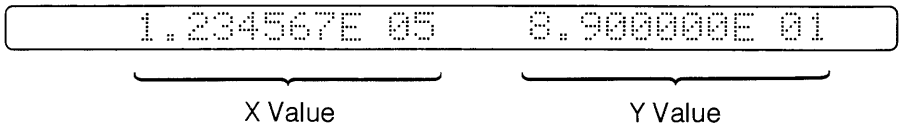


Figure 5-2. Interface Test Program 1

Table 5-1. Test Program 1 Results

Configuration Switch Position		Display	
S3	S2	X	Y
1234	1234567		
0000	0000000	1.234567E 05	8.90000E 01
0000	1000000	4.267000E 03	-9.153000E 03
0111	0000000	-1.234567E 05	9.000000E 00
0111	1000000	-4.267000E 03	9.150001E 03
0000	0001111	1.234567E 05	8.900000E 01
0000	0111100	1.234567E 05	8.900000E 01

Where: 1 = Switch ON
0 = Switch OFF

HPL

```
0: dim A$[20],B$[20]
1: ""→A$→B$
2: fmt ↓wtc 3,32↓wtc 3
3: fmt 2c16↓wrt 0,A$,B$
4: stp ↓gto 1
5: end
```

BASIC

```
10   DIM A$[20],B$[20]
20   A$=B$=""
30   WRITE IO 3,5;32
40   ENTER 3;A$,B$
50   DISP A$,B$
60   STOP
70   GOTO 30
80   END
```

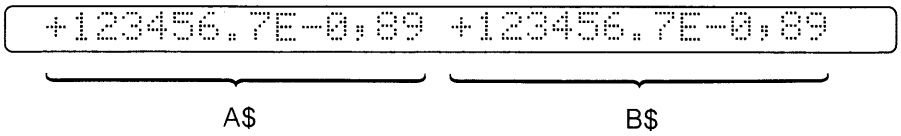


Figure 5-3. Interface Test Program 2

Table 5-2. Test Program 2 Results

Configuration Switch Position		Display	
S3 1234	S2 1234567	A$	B$
0000	0000000	+123456.7E-0,89	+123456.7E-0,89
0000	1000000	+4267,-9153.E80	+4267,-9153.E80
1000	0000000	-E-,+	908E+.,06
1000	1000000	-4+98,+6E	,0E0.
0111	0000000	-123456.7E+0,89	-123456.7E+0,89
1111	0000000	+E-,+	908E-.,86
1111	1110011	++-98,-6E	,0E8.
0000	0001111	+123456.7E-0,89	+123456.7E-0,89
0000	0111100	+123456.7E-0,89	+123456.7E-0,89

Where: 1 = Switch ON
0 = Switch OFF

Troubleshooting

To make the following tests or checks it will be necessary to remove the case from the interface cirucit boards. To do this, remove the screws from the sides of the interface. Use the Extender Board to reconnect the interface to the computer.

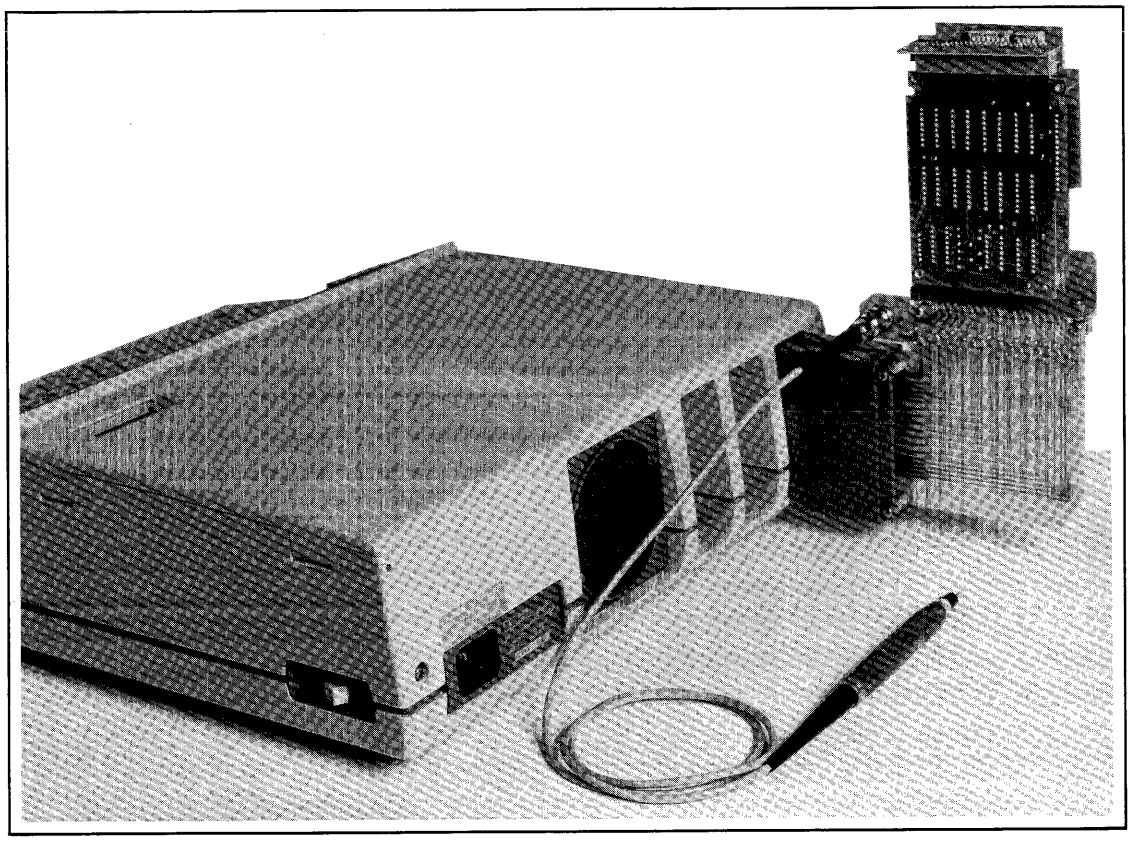


Figure 5-4. Extender Board Installation

Procedure

1. If the interface fails the test programs (refer to Interface Operational Test) check the select-code switch setting (the programs specify select code 3). Also, rotate the select-code switch back and forth to ensure proper switch contact (the switch may be intermittent).
2. If the program runs but the data is not correct start the program and:

    a. Check the output of each data selector, (pins 5 and 6 of U4 through U11). Each output should change states at least once during each data input cycle.

    b. Check the outputs of U1. All outputs should change states.

    c. Check the outputs of U4 (the BCD to ASCII converter). None of the computer data-input lines (IO 0-IO 7) should be held low continually.

3. If the program does not run at all, check the control logic in the following order (refer to the Theory of Operations).

   a. Interface select-code decoder
   b. Command Decoder
   c. Sample Control Circuit

Broken Trace Repair

If one or more traces are open or have high resistance, the trace should be bridged using insulated wire on the back of the boards where possible. Note - the boards are of multi-layer construction and, therefore, require good soldering technique to prevent damage.

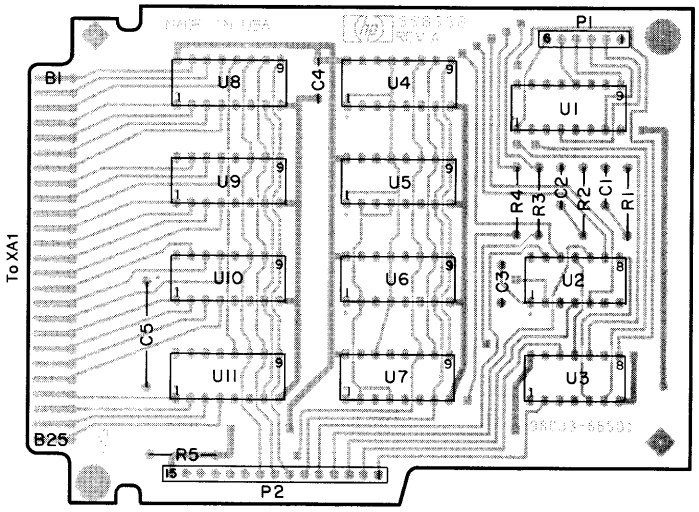
> CAUTION
> TO HELP PREVENT DAMAGE TO THE CIRCUIT BOARDS USE A LOW-TEMPERATURE SOLDERING IRON WHEN MAKING REPAIRS OR REPLACING PARTS.

Replaceable Parts List

Table 5-3. Replaceable Parts

REFERENCE DESIGNATOR	-hp- PART NO.		TQ	DESCRIPTION	MFR.	MFR. PART NO.
A1	**98033-66501**			**Multiplexer Board**		
C1,C2	0160-2964			C: fxd, .01μf 25V		
C3,C4	0160-2605			C: fxd, .02μf 25V		
C5	0180-0106			C: fxd, 60μf 6V		
P1,P2	1251-4226			Conn. 36 Pin		
R1,R2	0603-2225			R: fxd. 2.2k 5%		
R3,R4	0683-4705			R: fxd 47ohm 5%		
R5	0683-1025			R: fxd 1k 5%		
U1	1820-1438			IC: 74LS257N		
U2	1820-1211			IC: 74LS86N		
U3	1820-1416			IC: 74LS14N		
U4 thru U11	1820-1298			IC: 74LS251		
A2	**98033-66502**			**Control Board**		
C1	0180-0106			C: fxd 60μf 6V		
C2,C3	0160-2605			C: fxd .02μf 25V		
R1 thru R4	0683-2225			R: fxd 2.2k 5%		
R5,R6	0683-1035			R: fxd 10k 5%		
R7,R9	0683-2225			R: fxd 2.2k 5%		
R8	0683-1025			R: fxd 1k 5%		
R10	1810-0183			R: fxd – Network		
S1	3100-3364			Switch, Hex		
S2	3101-2152			Switch – DIP 7PST		
S3	3101-2160			Switch – DIP 4PST		
U1	1820-1206			IC: 74LS27		
U2	1820-1198			IC: 74LS03		
U3	1820-1297			IC: 74LS266		
U4	1816-0823			IC: 74S188		
U5,U16	1820-1202			IC: 74LS10		
U6	1820-1199			IC: 74LS04		
U7	1820-1197			IC: 74LS00		
U8	1820-1492			IC: 74LS368		
U9	1820-0514			IC: 7426		
U10,U17	1820-1112			IC: 74LS74		
U11	1820-1144			IC: 74LS02		
U12	1820-1201			IC: 74LS08		
U13	1820-1470			IC: 74LS157		
U14	1820-1194			IC: 74LS193		
U15	1820-1211			IC: 74LS86		
XA1P1	1251-4215			Conn. 6 Pin		
XA1P2	1251-4217			Conn. 15 Pin		
				Rear Housing		
	5040-7803			Case – Left		
	5040-7855			Case – Right		
	98033-61601			Molded Cable and Conn.		
	5040-8014			Molded Cable		
	1251-4147			Conn. 2 × 25		
	0590-0663			Nut-lock 4-40		
	2200-0510			Screw Mach 4-40		
				Front Housing		
	5040-7801			Case – Left		
	5040-7802			Case – Right		
	1480-0292			Pin – Dwl		
	5040-7836			Spring-latch		
	2200-0536			Screw 4-40 × .44		

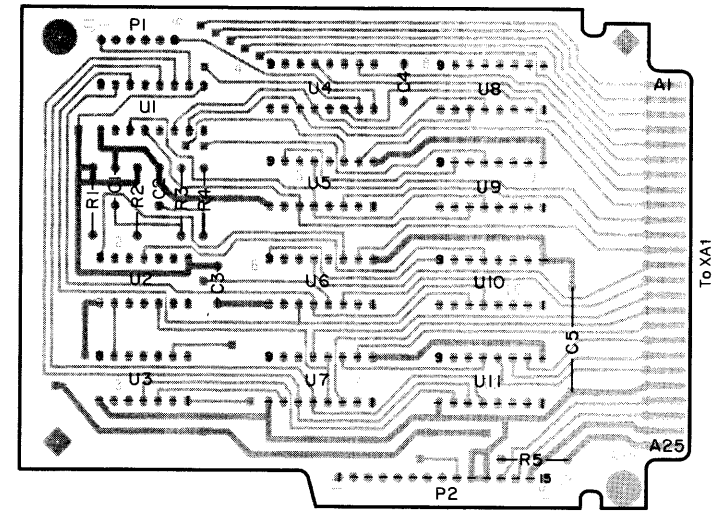
Component Locators



COMPONENT SIDE

A1

-hp- Part No. 98033-66501 Rev A

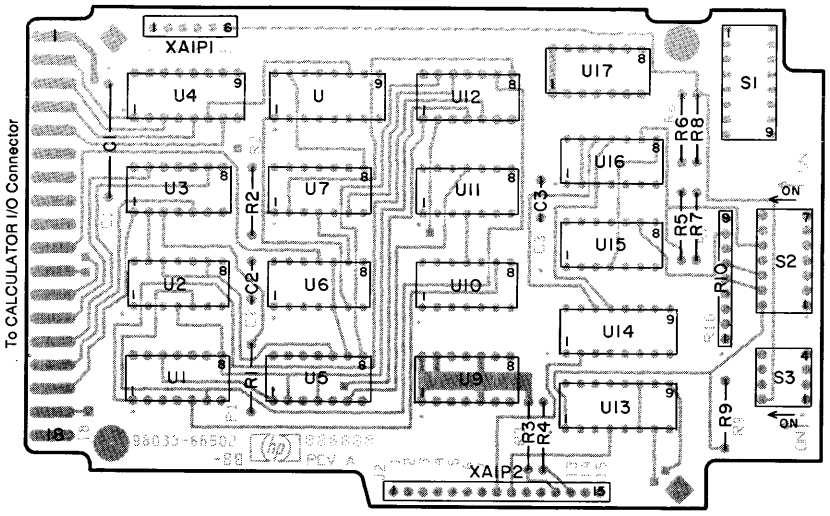


98033A-L-50862

CIRCUIT SIDE

A1

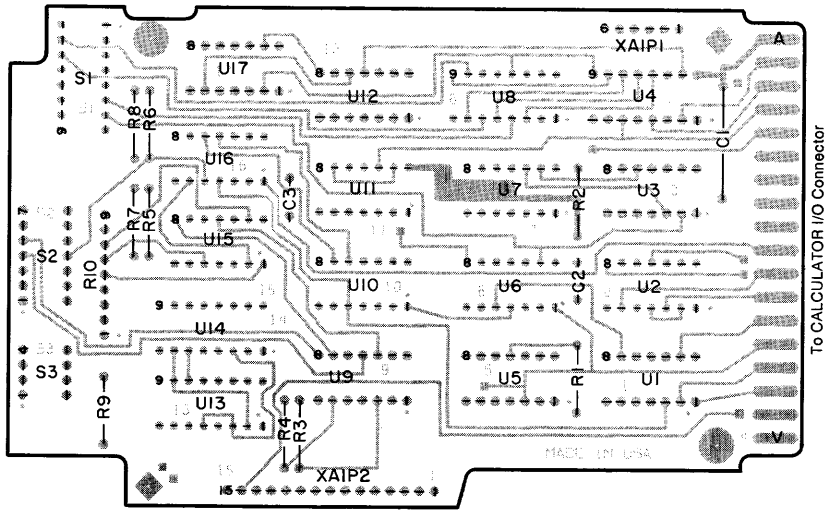
-hp- Part No. 98033-66501 Rev A



COMPONENT SIDE

A2

-hp- Part No. 98033-66502 Rev A



CIRCUIT SIDE

A2

-hp- Part No. 98033-66502 Rev A

98033A-L-50862

Interface Cable Wiring

Control

Mnemonic	Wire Color
CTLA	8
DFLGA	918
CTLB	98
DFLGB	928
GND	9
+5v ref	938
SHIELD*	NC

*The shield (and drain wire) should not be connected to anything at the peripheral end.

Standard Format

Data Field	Significance	Wire Color Code D (8)	C (4)	B (2)	A (1)
Sgn 1	Mantissa Sign	-	-	-	916
D1	Mantissa Digit 1	3	2	1	0
D2	Mantissa Digit 2	7	6	5	4
D3	Mantissa Digit 3	93	92	91	90
D4	Mantissa Digit 4	97	96	95	94
D5	Mantissa Digit 5	904	903	902	901
D6	Mantissa Digit 6	908	907	906	905
D7	Mantissa Digit 7	915	914	913	912
D8	Mantissa Digit 8	926	925	924	923
(E)	Enter Exponent*	-	-	-	-
Sgn 2	Exponent Sign	-	-	-	917
D9	Exponent Digit	937	936	935	934
(,)	End of Value*	-	-	-	-
(O.L.)	Overload	927	-	-	-
D10	Function Code	948	947	946	945
(L.F.)	End of Reading*	-	-	-	-

*These characters are generated by the interface.

Optional Format

Data Field	Significance	Wire Color Code D (8)	C (4)	B (2)	A (1)
Sgn 1	Value A Sign	-	-	-	916
D4	Value A Digit 1	97	96	95	94
D2	Value A Digit 2	7	6	5	4
D6	Value A Digit 3	908	907	906	905
D8	Value A Digit 4	926	925	924	923
(,)	End of Value A*	-	-	-	-
Sgn 2	Value B Sign	-	-	-	917
D10	Value B Digit 1	948	947	946	945
D1	Value B Digit 2	3	2	1	0
D5	Value B Digit 3	904	903	902	901
D3	Value B Digit 4	93	92	91	90
D7	Value B Digit 5	915	914	913	912
(E)	Enter Exponent*	-	-	-	-
(O.L.)	Overload A	927	-	-	-
D9	Overload B	937	936	935	934
(L.F.)	End of Reading*	-	-	-	-

*These characters are generated by the interface.

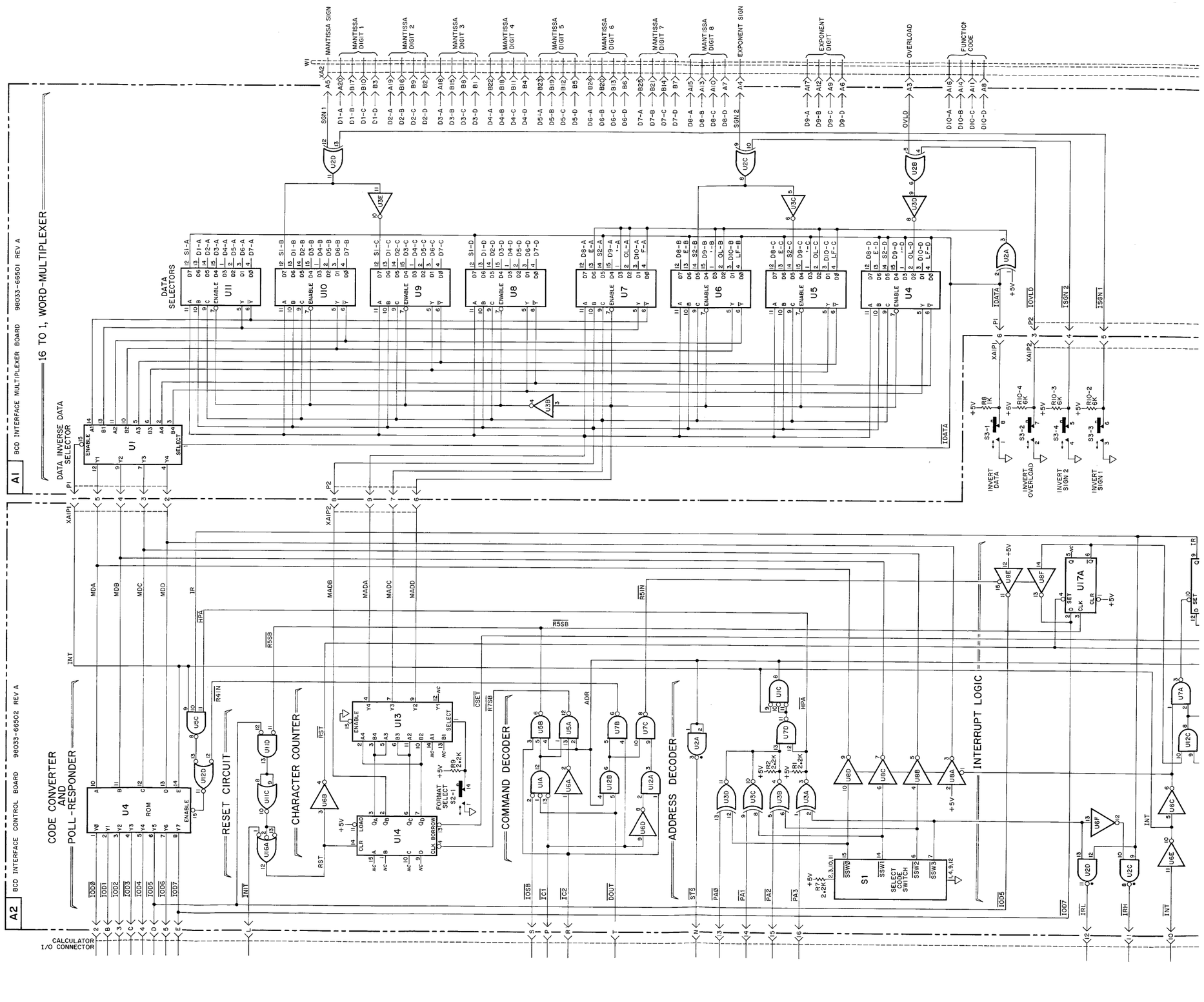


Figure 5-5. 98033A BCD Interface Schematic

98033A BCD Interface

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